(5,800,858) under 35 U.S.C. § 103. Applicants respectfully traverse.

Arbach et al. describes a system in which two electroactive bodies, consisting of different materials that have different redox potentials, are attached on top of each other and are subsequently structured. This is followed by seeding and separating the metal in the structured regions.

Contrary thereto, according to the claimed invention, a first insulation layer is applied on a substrate, and then the first insulation layer is activated using an activator. A second insulation layer is applied on the first insulation layer that is activated using the activator. The second insulation layer is then structured. The first insulation layer is subsequently seeded and metalized.

According to Arbach et al., the activation of the first electroactive body, i.e. the first electroactive layer does not take place before the second electroactive layer is applied thereon. For this reason they teach that different materials are necessary which have different redox potentials.

According to the invention, however, it is possible to use the same material for both insulation layers due to the fact that the first insulation layer is activated using an activator

before the second insulation layer is applied thereon, which achieves a greatly improved adhesion of the two layers with each other.

Due to this possibility of using the same material for both insulation layers, a greatly simplified production process as compared to the production process of Arbach et al. is achieved, because the process line does not need to be adjusted to several different electroactive layers and insulation layers consisting of different materials.

This leads to greatly reduced costs of the metal deposition in the inventive method as compared to the method taught in Arbach et al.

Such a process is not even hinted at in Angelopoulos et al.. According to Angelopoulos et al., the entire insulation layer is seeded and a photo-layer is necessary, which must be removed after performing the process that has the advantages as described in the introductory specification, specifically, a particle formation is caused by stripping the resist that leads to a reduced yield.

Angelopoulus et al. can thus also not give any information towards the claimed method.

Such information can also not be found in Bickford et al., due to the fact that according to Bickford et al. only an insulation layer is present which is structured. Applicants respectfully believe that Bickford et al. is not even relevant for the object of the present invention.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 4. Claim 4 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 4-7 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, he is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and

Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Mark P. Weichselbaum
Reg. No. 43,248

For Applicants

MPW:cgm

June 6, 2002

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

GR 01 P 1583

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klaus Lowack et al.

Applic. No. : 09/817,963

Filed : March 27, 2001

Title : Method For The Metalization Of An Insulator And/Or A Dielectric

Examiner : Brian K. Talbot

Group Art Unit : 1762

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On page 3, lines 18-21:

The object and subject of the invention are achieved by a process for the metallization of at least one insulating layer of an electronic or microelectronic component, whose layer thickness is at most 50 [Fm] µm, wherein firstly

On page 5, lines 13-14:

The thickness of the insulating layer is preferably between 0.05 and 50 [Fm] µm, particularly preferably between 0.1 and 20 [Fm] µm.